Low Power Converters for High Output Voltages

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Abstract
The paper presents circuit topologies for medium voltage converters and investigates their suitability for high voltage low power applications with up to 4 MVA. For an example of an inverter for 6 kV motor voltage the four level floating capacitor topology was chosen. Advantages of this topology are the balanced power dissipation of the power semiconductor devices and direct voltage clamping of each power device. Details of the motor inverter design are presented.

Introduction
The availability of high voltage turn-off power semiconductor devices with 6.5 and 10 kV blocking capability opens the door for medium voltage inverters for 6 kV motor voltage without direct series connection of power devices. Due to the insulation stress of the motor windings two level inverters can not be recommended for medium voltage applications. Two well established medium voltage circuit topologies are the neutral point clamped three level inverter and the floating capacitor multilevel inverter [1]. Goal is to find the best solution for 6 kV motor voltage in the power range up to approximately 4 MVA.

Choice of circuit topology and type of semiconductor for 6 kV inverter
For any comparison of power semiconductor devices to be used in medium voltage converters the converter topology has also to be taken into account. Multilevel topologies such as three level neutral...
point clamped and four level floating capacitor topologies are commonly preferred for medium voltage converters [2]. Advantages are the intelligent series connection of power devices and an output voltage waveform without steps of the amount of $U_d$. The following discussion presents features of both topologies.

Fig. 1 shows a schematic diagram of a three level neutral point clamped inverter phase. Main advantage of this topology is the series connection of power semiconductor devices with good controllable voltage sharing by usage of redundant switching states. Unbalanced power dissipation of power semiconductor devices depending on the load angle and the degree of modulation have to be taken into account for the inverter design.

Fig. 2: Schematic diagram of a 4 level floating capacitor inverter phase.

The schematic diagram of a four level floating capacitor inverter phase is shown in Fig. 2. Main advantages are the balanced power dissipation of the power semiconductor devices and direct voltage clamping of each power device. Optionally the number of levels can be extended for higher motor voltages or to improve the THD of the output current. Disadvantages are high current stress of floating capacitors and the impact of pulse frequency and output current on the floating capacitor dimensioning. For this reason this topology is best suited for low to medium power up to approximately 4 MVA and high voltages.

Due to the circuit topology with floating capacitors power semiconductors requiring turn-on snubbers can not be used. The introduction of a choke in the commutation path would cause oscillations with the risk of overvoltages. Because of the modular design of a floating capacitor commutation cell representing a stage of the inverter phase direct series connection of power devices can be avoided. For this reason module type IGBT devices are preferred.

For the neutral point clamp inverter higher motor voltages can be achieved by direct series connection of power semiconductor devices. An extension to a higher number of levels is not useful because the voltage sharing can not be controlled by redundant switching states.

Inverter design

The commutation cell of the 6 kV inverter is mechanical identical to the existing 4.16 kV design (Fig. 3). Nominal IGBT blocking voltage has been changed from 4.5 to 6.5 kV, capacitor voltage rating has been adapted, too. Insulation design and commutation inductance of the existing design was prepared for the higher voltage level. The patented air isolated low inductive commutation circuit design can easily be designed for even higher voltages with no partial discharge problems. Commutation cell inductance in the
range of much less than 150 nH for the circuit including two floating power capacitors and two single IGBT switches has been verified by measurements.

![Image](https://via.placeholder.com/150)

Fig. 3: Floating capacitor inverter commutation circuit with low stray inductance.

The inverter design is based on the design of the existing inverter with 4.16 kV voltage rating. Some improvements have been done. Capacitor sizing is an important issue because of the increased capacitances at lower switching frequencies. Following ratios had to take into account for the capacity of the floating capacitors for equal voltage ripple percentage:

\[ C \sim I \]
\[ C \sim 1/V^2 \]
\[ C \sim 1/f_{\text{pulse}} \]

![Image](https://via.placeholder.com/150)

Fig. 4: Low inductive capacitor module.
Capacitance for unit of power (kVA) is decreasing with $1/V^2$ based on equal switching frequency. Capacitor size $C/2V^2$ stays unchanged for unchanged power rating, but is increasing with lowered switching frequency by $1/f_{\text{switching}}$. For reasons of modularity capacitor banks based on simple cylindrical capacitors have been tested to replace huge low inductive non-standard power capacitors. The parasitic inductance of these banks can be designed by paralleling small cylinders. In Fig. 4 a capacitor bank 360 $\mu$F / 4.5 kV consisting of 8 cylindrical capacitors with low inductive terminals to top and bottom connected IGBT-modules is shown. This approach allows a cost effective scalable solution for different power ratings.

The parasitic inductance of the inner commutation circuit including 2 IGBT modules 600 A / 6.5 kV and this capacitor bank has a measured value of 75 nH (see measurement results below). For the outer circuits including the required second capacitor bank the commutation inductance becomes 100 nH.

The 6.5 kV IGBTs, used as power switches in the inverter circuit are controlled by a new gate driver. Measurements have been made with 600 A / 6500 V IGBT modules from 3 different manufacturers.

In Fig. 5 collector current and voltage waveforms for turn-on and turn-off at IC = 1000 A, Ud = 4400V and $T_j = 125^\circ C$ are shown for the CM600HG-130H (Mitsubishi). We see the expected shapes. The low turn-off overvoltage peak of 200 V is a result of the low commutation inductance for switching with recommended gate conditions.

The first new main feature of the gate drive is the short circuit detection method, avoiding the disadvantages of the desaturation detection method with slow switching high voltage IGBT’s. The problem of state of the art desaturation detection in high voltage devices clearly can be seen in the turn-on voltage shape in Fig. 5. It takes 10 $\mu$s from start of rise of collector current till the forward voltage drop falls in the range of volts. On the other side within this 10 $\mu$s the short circuit must be turned off. One possibility for faster short circuit detection is based on checking more then simply one point. The novel gate drive is detecting the magnetic field of currents in the commutation circuit and by this detects short circuit states much faster then conventional methods.
a) $U_d = 2.5 \text{ kV}$  

Fig. 6: Type I short circuit turn-off.

In Fig. 6 short circuit turn-off waveforms for short circuit type I, when the IGBT turns on into the short circuit, are shown for $U_d = 2500 \text{ V}$ and $U_d = 4400 \text{ V}$. Depending on the junction temperature the short circuit peak current of the device under test reaches a value of $5.8 \text{ kA}$ and $6.3 \text{ kA}$ within 2 to 3 $\mu$s after current rising. Within maximum 3 microseconds after reaching the peak current the short circuit is turned off. As a result the huge energy dissipated in the device during short circuit is much less then for conventional short circuit turn off within 10 $\mu$s. The low overvoltage peak is contributed to the gate drive and the low inductive design of the commutation circuit.

For short circuit type II, when the short circuit current is rising in the saturated IGBT structure, the detection is even faster.

In Fig. 7 short circuit turn-off waveforms for short circuit type II with FZ600R65KF1 (eupec) are displayed for $U_d = 2.5 \text{ kV}$ and $U_d = 4.4 \text{ kV}$. Here the short circuit peak current is reached within maximum 2 $\mu$s. Again within much less than 10 $\mu$s the current is completely turned off.

The second new feature of the gate drive is the measurement of analogue values and the data transfer to the control system in the existing fibre optic feedback channel. In this channel signals like currents, voltages, temperatures or others can be transmitted. This feature can be used for protection, like heat sink temperature observation, IGBT overvoltage protection or in multilevel topologies for floating capacitor voltage control in conjunction with synchronous pulse patterns.
Based on the measurement values of the non conducting IGBT’s the floating capacitor voltages can be calculated. The redundant information based on 3 IGBT voltages per phase and the independent measured dc-voltage Ud is used for data plausibility check. The capacitor voltage control is implemented in the pulse pattern generator. The achieved degree of freedom makes the floating capacitor inverter topology as flexible as others in terms of possible control strategies. Summarising we can observe, that the new gate drive makes the inverter more flexible and even more robust with no additional hardware expenditure.

**Drive ratings**

This section gives an overview of the achievable drive nominal and overload ratings for a 6 kV four level floating capacitor motor inverter with 6.5 kV/600 A IGBT modules. Design approaches for forced air and liquid cooling are investigated. Due to the high specific switching losses of semiconductor devices with high blocking capability a low pulse frequency of 500 Hz is assumed. For both design approaches high performance heat sinks were considered. In case of forced air cooling with maximum 40 °C ambient temperature the nominal inverter output current will be 250 A with 10 % overload capability for 60 s with a repetition rate of 600 s. The same kind of IGBT module mounted on a liquid cooled heat sink is able to deliver a nominal motor current of 400 A. Main reason for the increased output current in case of liquid cooling is the low thermal steady state resistance of such kind of heat sink. Due to the main application field of power inverters in adjustable speed drives the power dissipation of semiconductors is not constant over time. For this reason the transient thermal impedance of the heat sink and their side effects have to be taken into account. Fig. 8 shows derating curves for the inverter output current versus output frequency. Advantage of the higher weight of the heat sink for forced air cooling is the higher thermal capacity. In conjunction with their thermal resistance a thermal low pass filter is formed, damping the junction temperature curve of power semiconductors in case of low frequencies of the output current and in case of power cycles.

![Fig. 8: Inverter output current vs. output frequency for the water cooled (gray lines) and the air cooled (black lines) 6 kV inverter design. Parameters: \( f_p = 500 \text{ Hz}; \ T_{\text{coolant}} = 40^\circ\text{C}; \ T_{j(\text{max})} = 120^\circ\text{C}; \Delta T_{j(\text{max})} = 25 \text{ K}. \)](image)

![Fig 9: Calculated temperatures of IGBT (black line) and FWD (gray line) vs. time of the air cooled inverter at \( I_{\text{out}} = 240 \text{ A} \) and \( f_{\text{out}} = 2.8 \text{ Hz}. \) Parameters: see Fig. 8.](image)

Side effect of the small thermal capacitance of the liquid cooled inverter is an output current derating for motor frequencies below approximately 8 Hz. For the assumed air cooled inverter an output current derating is required below 4 Hz. For smaller output frequencies two derating curves have to be considered. The solid curves show the deratings for continuous operation. For this curves the junction peak temperature \( T_{j(\text{max})} \) and the junction temperature ripple \( \Delta T_{j(\text{max})} \) is below a specified value. For
discontinuous operation higher junction temperature ripples below the specified maximum junction temperature are possible. This operation mode causes power cycles reducing the lifetime of IGBT modules. For a given operating point of the air cooled inverter the curves of the IGBT and freewheeling diode junction temperatures are shown in Fig. 9. In this point the specified maximum junction temperature of 120°C and the specified maximum junction temperature of ripple 25 K are reached.

![Fig. 10](image1.png)  
**Fig. 10:** Calculated junction temperatures of forced air cooled motor inverter at nominal load / 10 % overload load cycle. Single switch IGBT module 6.5 kV / 600 A.  
Parameters: \( I_{\text{out}} = 250 \text{ A}/275 \text{ A} \ (540 \text{ s} / 60 \text{ s}) \); \( f_p = 500 \text{ Hz} \); \( T_{\text{coolant}} = 40^\circ \text{C} \); \( \cos \phi = 1 \); \( m = 1.15 \).

![Fig. 11](image2.png)  
**Fig. 11:** Calculated junction temperatures of liquid cooled motor inverter at nominal load / 10 % overload load cycle. Single switch IGBT module 6.5 kV / 600 A.  
Parameters: \( I_{\text{out}} = 400 \text{ A}/440 \text{ A} \ (540 \text{ s} / 60 \text{ s}) \); \( f_p = 500 \text{ Hz} \); \( T_{\text{coolant}} = 40^\circ \text{C} \); \( \cos \phi = 1 \); \( m = 1.15 \).

Calculated junction temperatures for a standard load cycle 60 s/600 s with 10 % overload are shown in Fig. 10 for the air cooled design and in Fig. 11 for the liquid cooled inverter. Dimensioning has been done for an average junction temperature of \( T_{\text{j}}(\text{av}) = 110^\circ \text{C} \) at nominal output current and maximum coolant temperature. Due to the larger thermal capacitance of the air cooled heat sink the junction temperature ripple is smaller as for the liquid cooled heat sink. It can also be seen very clearly that for the liquid cooled inverter an overload over 30 s behaves like a steady state load for the IGBT module.

Conclusions

A three level neutral point clamp and a four level floating capacitor inverter topology have been investigated regarding low to medium power output with up to 4 MVA and high motor voltages. For a design example of an inverter for 6 kV motor voltage the four level floating topology with 6.5 kV module type IGBT power semiconductor devices was preferred. Advantages of this topology are balanced power dissipation of power semiconductors and an extendable modular design for higher voltages. Design details have been discussed. The comparison between a design for forced air cooling and a second design for liquid cooling shows the increased sensitivity of the liquid cooled design for power cycles and low output frequencies. Reason is the comparable small thermal capacitance of the liquid cooled heat sinks.

References