Programm des 24. Workshops „Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen” (MBMV 2021)

TU München - Virtuelles Event, 18.-19. März 2021

Bild: Astrid Eckert / TUM

The MBMV Workshop of the GMM/ITG/GI-Fachgruppen 3 und 4 is a forum to discuss trends in modeling, verification, and generation of embedded systems, software and hardware. While the workshop language is German and English, most of the program this year will be in English.

This year, due to the special situation, MBMV is held as a virtual online event instead of a local event in Munich. Nevertheless, we are excited that the interest in MBMV stayed high shown in a program with five technical sessions covering two days. To adapt for the situation, MBMV introduced a new contribution this year: the demonstration of open source software tools in the domain of system modeling and verification, which can be perfectly presented in an online format. The demonstration will happen in two afternoon sessions, which shows the new trend of Open Source EDA gaining more and more traction.

Finally, we are especially excited to have three keynotes from speakers from Infineon Technologies AG, Bosch Research and Intel to present their work and vision for research in the fields of MBMV for the coming years.

I invite you to join MBMV online and am looking forward to an exciting event with you this year.

Best wishes,

Daniel Mueller-Gritschneder, program committee head 2021

Program Highlights

Thursday Morning Keynote (9:00)

Model Driven Architecture applied to Industrial SoC-Design
Prof. Wolfgang Ecker, Distinguished Engineer, Infineon Technologies AG

BIO: Wolfgang Ecker is Distinguished Engineer at Infineon and Adjunct Professor at Technical University of Munich. He is author of over 200 papers on modeling and design automation, received 5 awards for his papers, and was granted with the German EDA achievement award. Wolfgang is member of Acatech, the German Academy of Science and Engineering and the AI commission of inquiry of the German Parliament. Wolfgang Ecker also leads the Infineon Deep Learning internal think tank, the development of AI-based EDA methods and the implementation of specialized RISCV cores.

Thursday Afternoon Keynote (13:30)

Simulating Vehicle Computer Systems
Dr. Dirk Ziegenbein - Chief Expert, Robert Bosch GmbH

Abstract: Driven by new functionality and applications (like automated driving and vehicle-to-X-connectvity), the automotive industry is introducing centralized Eletric/Electronic architectures featuring powerful vehicle computers. This poses new challenges for the development process and particularly also for the HW/SW integration and validation. This talk will give insight into current approaches and upcoming research challenges for modelling and simulation of automotive applications.

BIO: Dirk Ziegenbein is chief expert for cyber-physical systems engineering and leads a group of 20 researchers developing methods and technologies for software systems engineering at Bosch Corporate Research in Stuttgart, Germany. Dirk received a Master's degree from Virginia Tech and a Ph.D. from Technical University of Braunschweig for his dissertation on modeling and design of embedded systems. He held several positions in R&D (software component technology, scheduling analysis, software architectures for multi-cores, autonomous systems design) and product management (embedded software engineering tools). Additionally, Dirk serves in various technical program committees including DAC and DATE.

Friday Morning Keynote (9:00)

Scaling Virtual Platforms across Use Cases and the Product Lifecycle
Dr. Jakob Engblom, Product manager for the Simics virtual platform tool, Intel

Abstract: Virtual platforms and related simulation technologies are key to the efficient design, development, deployment, and support of computer systems new and old. In this talk, Jakob Engblom from Intel will talk about the uses of virtual platforms that he has seen over the years - from computer architecture, to pre-silicon firmware and software development, to ecosystem enablement, to digital twins, all the way to supporting obsolete hardware platforms. The scale of a VP can range from a single processor core with some memory all the way up to networks of machines and racks, and the model for each component part can also vary in depth of detail and its abstraction level. The exact configuration and models used depend on the use case, and it is common to have multiple models for each subsystem.

Bio: Dr. Jakob Engblom works at Intel in Stockholm, Sweden, as a product manager for the Simics virtual platform tool and simulation evangelist. He has been working with Simics virtual platforms since 2002, first at Virtutech, then Wind River, and now at Intel. Over the years, he has published and presented more than a hundred papers and talks at various conferences and workshops, on topics including virtual platforms, system simulation, debugging, programming, and embedded systems. Jakob got his first computer in the early 1980s and never looked back, eventually getting a PhD in Computer Systems from Uppsala University, Sweden.

Program on Thursday, March 18, 2021

8:45	*Welcome (Prof. Daniel Mueller-Gritschneder, TU Munich)*
9:00	**Thursday Morning Keynote** Model Driven Architecture applied to Industrial SoC-Design Prof. Wolfgang Ecker, Distinguished Engineer, Infineon Technologies AG
9:45	**Talk Session: Better Software and Systems**
9:45	Benchmarking SMT Solvers on Automotive Code (Lukas Mentel[1], Karsten Scheibler[1], Felix Winterer[2], Bernd Becker[2], Tino Teige[1], [1]*BTC Embedded Systems AG,* [2]*Albert-Ludwigs-University Freiburg*)
10:05	VP-based DIFT for Embedded Binaries: A RISC-V Case Study (Pascal Pieper[3], Vladimir Herdt[1,3], Daniel Grosse[2,3], Rolf Drechsler[1,3], [1]*University of Bremen,* [2] *Johannes Kepler University Linz,* [3]*DFKI Bremen*)
10:25	Ontology Design for Microelectronics with Roadmapping (Frank Wawrzik, Christoph Grimm, *TU Kaiserslautern*)
10:45	*Break*
11:00	**Talk Session: Getting Performance Analysis right**
11:00	A Matter of Overhead - Response-Time Analysis of Hard Real-Time Systems in Theory and Practice (Max Brand[1], Albrecht Mayer[1], Frank Slomka[2], [1]*Infineon Technologies,* [2]*Ulm University*)
11:20	Exploration of DDR5 with the Open Source Simulator DRAMSys (Lukas Steiner[1], Matthias Jung[2] and Norbert Wehn[1], [1]*TU Kaiserslautern,* [2]*Fraunhofer IESE*)
11:40	Comprehensive modeling and evaluation of Network-on-Chip performability (Jie Hou and Martin Radetzki, *University of Stuttgart*)
12:00	Decision Tree-based Throughput Estimation to Accelerate Design Space Exploration for Multi-Core Applications (Martin Letras, Joachim Falk, Jürgen Teich, *Friedrich-Alexander University Erlangen-Nuremberg*)
12:20	*Lunch break*
13:30	**Thursday Afternoon Keynote** Simulating Vehicle Computer Systems Dr. Dirk Ziegenbein - Chief Expert, Robert Bosch GmbH
14:15	**Talk Session: Methodology and Solvers – Deep Dive**
14:15	ICP and IC3 with Stronger Generalization (Felix Winterer[2], Tobias Seufert[2], Karsten Scheibler[1], Tino Teige[1], Christoph Scholl[2] and Bernd Becker[2], [1]*BTC Embedded Systems AG,* [2]*Albert-Ludwigs-University Freiburg*)
14:35	Extended Abstract: Viability of Decision Trees for Learning Models of Systems (Swantje Plambeck, Lutz Schammer and Görschwin Fey, *Hamburg University of Technology*)
14:55	Stärkung deterministischer Strategien für POMDPs (Leonore Winterer[1], Ralf Wimmer[1,2], Nils Jansen[3], Bernd Becker[1], [1]*Albert-Ludwigs-University Freiburg*, [2]*Concept Engineering GmbH,* [3]*Radboud University*)
15:15	*Break*
15:30	**SW Demos on Open Source Simulation on Modeling Tools**
15:30	Bewertung und Analyse heterogener Hard- und Software Systeme der nächsten Generation (Harald Mackamul and Joerg Tessmer, *Robert Bosch GmbH*)
16:00	Der Open Source DRAM Simulator DRAMSys4.0 (Matthias Jung[2] Lukas Steiner[1], Norbert Wehn[1], [1]*TU Kaiserslautern,* [2]*Fraunhofer IESE*)
16:30	QEMU zur Simulation von Worst-Case-Ausführungszeiten (Peer Adelt, Bastian Koppelmann, Wolfgang Mueller and Christoph Scheytt, *Paderborn University / Heinz Nixdorf Institute*)
17:00	Sitzung der GMM/ITG/GI-Fachgruppen 3 und 4

Program on Friday, March 19, 2021

8:45	*Welcome*
9:00	**Friday Morning Keynote** Scaling Virtual Platforms across Use Cases and the Product Lifecycle Dr. Jakob Engblom, Product manager for the Simics virtual platform tool, Intel
9:45	**Talk Session: RISC-V and Agility**
9:45	Constrained Random Verification for RISC-V: Overview, Evaluation and Discussion (Sallar Ahmadi-Pour[1], Vladimir Herdt[1,2] and Rolf Drechsler[1,2], [1]*University of Bremen,*[2]*DFKI Bremen*)
10:05	Register and Instruction Coverage Analysis for Different RISC-V ISA Configurations (Peer Adelt, Bastian Koppelmann, Wolfgang Mueller and Christoph Scheytt, *Paderborn University / Heinz Nixdorf Institute*)
10:25	APPEL - AGILA ProPErty and Dependency Description Language (Christoph Grimm[1], Frank Wawrzik[2], Alexander Louis-Ferdinand Jung[3], Konstantin Lübeck[3], Johannes Koch[1], Sebastian Post[1] and Oliver Bringmann[2], [1]*TU Kaiserslautern,* [2]*University of Kaiserslautern,* [3]*Eberhard Karls-Universität Tübingen*)
10:45	*Break*
11:00	**Talk Session: Generators, Compilers, Simulators**
11:00	Extending Verilator to Enable Fault Simulation (Endri Kaja, Nicolas Ojeda Leon, Michael Werner, Bogdan-Andrei Tabacaru, Keerthikumara Devarajegowda and Wolfgang Ecker, *Infineon Technologies AG*)
11:20	Approximate Computing Extensions for the Clash HDL Compiler (Oliver Keszocze and Michael Kießling, *Friedrich-Alexander-Universität Erlangen-Nürnberg*)
11:40	On Self-Verifying DSL Generation for Embedded Systems Automation (Zhao Han, Shahzaib Qazi, Michael Werner, Keerthikumara Devarajegowda, Wolfgang Ecker, *Infineon Technologies)*
12:00	Operation Level Synthesis (Lucas Deutschmann, Johannes Schauß, Tobias Ludwig, Dominik Stoffel, Wolfgang Kunz, *Technische Universität Kaiserslautern*)
12:20	*Lunch Break*
13:00	**SW Demos on Open Source Verification Tools**
13:00	GenMul: Generating Architecturally Complex Multipliers to Challenge Formal Verification Tools (Alireza Mahzoon[1], Daniel Grosse[2,3] , Rolf Drechsler[1,3], [1]*University of Bremen,*[2] *Johannes Kepler University Linz,* [3]*DFKI Bremen*)
13:30	CHIPS: A Property Specification and Verification Framework for RISC-V based System-on-Chip (SoC) designs (Anton Paule[1] and Oliver Bringmann[2], [1]*FZI Forschungszentrum Informatik,* [2]*Eberhard Karls-Universität Tübingen)*
14:00	*Wrap-up*
14:15	*Ende*